AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-34. (cancelled)

35. (new) A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of said chip areas;

forming a plurality of electrode test pads on an uppermost surface of said first metal wiring layer for carrying out a provisional yield rate test;

subjecting said wafer to said provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by forming a second metal wiring layer on said first metal wiring layer when said wafer passes said provisional yield-rate test,

wherein a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate

test, and it is determined that said wafer has passed said provisional yield-rate test when said yield-rate exceeds a predetermined permissible rate.

36. (new) A production process as set forth in claim 35, wherein said first metal wiring layer is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second metal wiring layer is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request.

37. (new) The production process as set forth in claim 36, wherein said customized wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface of said second metal wiring layer, and wherein the electrode pads of said second metal wiring layer are arranged above the electrode pads of the first metal wiring layer with at least one insulating layer being intervened therebetween.

38. (new) A production process as set forth in claim 35, further comprising:

subjecting said wafer to a genuine yield-rate test in which it is examined whether each of the finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

finally processing said wafer when said wafer passes said genuine yield-rate test.

39. (new) A production process as set forth in claim 38, wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate.

40. (new) A production process as set forth in claim 38, wherein said second metal wiring layer has a plurality of electrode pads formed on an uppermost surface thereof, and said genuine yield-rate test is carried out, using the electrode pads of said second metal wiring layer.

41. (new) A production process as set forth in claim 40, wherein said first metal wiring layer is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on each of said chip areas, and said second metal wiring layer is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on said first metal wiring layer.

42. (new) The production process as set forth in claim 40, wherein the electrode pads of the second metal wiring layer

are vertically above the electrode pads of the first metal wiring layer.

43. (new) A process for producing a plurality of semiconductor devices on chip areas of a wafer, said process comprising:

forming a first metal wiring layer on each of the chip areas, said first metal wiring layer having a first test section;

performing a provisional yield-rate test using a respective first test section to determine whether each of said first metal wiring layer is acceptable or unacceptable; and

forming a second metal wiring layer on said first metal wiring layer when said wafer passes said provisional yield-rate test, said second metal wiring layer having a second test section that is different from and connected to said first metal wiring layer,

wherein said first metal wiring layer has a plurality of electrode pads formed on an uppermost surface thereof, for carrying out said provisional yield-rate test.

44. (new) The process as set forth in claim 43, further comprising:

performing a genuine yield-rate test using said second test section to determine whether each of said second metal wiring layer is acceptable or unacceptable to thereby find a yield-rate of acceptable finished semiconductor devices; and

processing said wafer when said wafer passes said genuine yield-rate test.

45. (previously presented) The process as set forth in claim 44, wherein said second metal wiring layer has a plurality of electrode pads formed on an uppermost surface thereof, said genuine yield-rate test being carried out using the electrode pads of said second metal wiring layer.

46. (previously presented) The process as set forth in claim 43,

wherein said step of forming said first metal wiring layer comprises forming a multi-layered wiring-arrangement section comprising at least two metal circuit pattern layers and at least one insulation layer alternately laminated on each of said chip areas, and

wherein said step of forming said second metal wiring layer comprises forming a multi-layered wiring-arrangement section comprising at least two metal circuit pattern layers and at least one insulation layer alternately laminated on said first metal wiring layer.

47. (new) The production process as set forth in claim 43, wherein the second test section is vertically above the first test section.

48. (new) A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, said production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of said chip areas, each said first metal wiring layer having a first test section electrically connected to an active region of a respective one of said chip areas;

subjecting said wafer to a provisional yield-rate test using said first test section to determine whether each of said semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by forming a second metal wiring layer on said first metal wiring layer when said wafer passes said provisional yield-rate test, each said second metal wiring layer having a second test section, different than said first test section, that is electrically connected to said active region of a corresponding one of said chip areas.

49. (new) A production process for producing a plurality of semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming at least one first metal wiring layer on each of said chip areas;

subjecting said wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable to thereby find a yield-rate of acceptable semi-finished semiconductor devices; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by at least one step of depositing and patterning a metal layer to form at least one second metal wiring layer over said at least one first metal wiring layer when said wafer passes said provisional yield-rate test.

50. (new) The production process as set forth in claim 49, wherein a plurality of electrode pads are formed on an uppermost surface of said first wiring layer, for carrying out said provisional yield rate test.